

- 3.0V to 3.8V power supply option
- Guaranteed AC parameters over temperature:
  - $f_{MAX} = 800\text{MHz}$
  - $< 200\text{ps}$  differential propagation delay (D to  $Q_{FB}$ )
  - $< 730\text{ps}$  differential propagation delay (D to  $Q_{HG}$ )
  - $< 250\text{ps}$   $t_r / t_f$
- Low-gain feedback path  $Q_{FB} = +10\text{V/V}$
- $V_{BB}$  reference output voltage
- Wide temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Available in 10-pin (3mm x 3mm) MSOP
- LVPECL/LVECL/CMOS compatible EN option



Precision Edge®

## DESCRIPTION

The SY89207L is a differential receiver amplifier optimized for crystal oscillator applications. The device includes an additional low differential gain (+10V/V) output stage ( $Q_{FB}$ ) ideal for feedback applications common in crystal oscillator gain blocks. The SY89207L is fully differential, with a bandwidth  $> 800\text{MHz}$  over temperature and voltage. For applications that require output disable control, a LVPECL/LVECL/CMOS compatible enable pin (EN) will force the differential output into a fixed logic state. The SY89207L also includes a  $V_{BB}$  reference voltage for single-ended or AC-coupled applications.

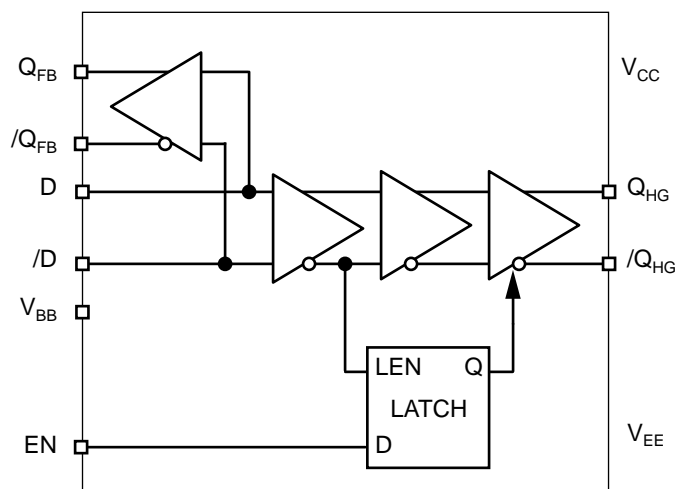
The SY89207L PECL logic is 100k ECL compatible. Operation is guaranteed over the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range and 3.3V nominal supply voltage range.

All support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

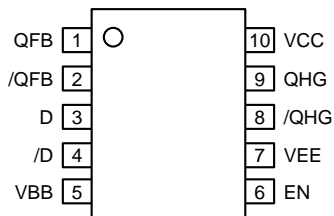
## APPLICATIONS

- Oscillator timing modules

## BLOCK DIAGRAM



**PACKAGE/ORDERING INFORMATION**



**10-Pin MSOP (K10-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89207LMI	K10-1	Industrial	SY89207L	Sn-Pb
SY89207LMITR <sup>(2)</sup>	K10-1	Industrial	SY89207L	Sn-Pb
SY89207LMG	K10-1	Industrial	SY89207L with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89207LMGTR <sup>(2)</sup>	K10-1	Industrial	SY89207L with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only.
2. Tape and Reel.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
1, 2	QFB, /QFB	Differential clock outputs for feedback path: Nominal DC gain +10.
3, 4	D, /D	LVPECL, LVECL differential inputs: Internal 75kΩ pull-down resistor.
5	VBB	V <sub>CC</sub> -1.32V reference voltage for single-ended inputs: It provides the switching reference for the input differential amplifier. When unused, it can be left open. For single-ended PECL applications connect V <sub>BB</sub> to /D input. For differential AC-coupled inputs, terminate each input with 50Ω to V <sub>BB</sub> as close to the input pins as possible. Always bypass the V <sub>BB</sub> pin with a 0.01μF capacitor to V <sub>CC</sub> .
6	EN	Enable: LVPECL/LVECL/CMOS compatible input control with internal 25kΩ pull-up resistor. It enables/disables the high-gain output (Q <sub>HG</sub> ). Default state is enabled, logic HIGH, if left floating. When EN pin is pulled to a logic LOW or GND, the Q <sub>HG</sub> output pair will be latched, as described in the "Truth Table." EN is synchronous so that the outputs will only be enabled/disabled when they are in the LOW state. Input threshold is V <sub>BB</sub> .
7	VEE	Negative power supply: For LVECL operation, connect to negative supply. For LVPECL operation, connect to GND.
8, 9	QHG, /QHG	Differential high-gain outputs: Nominal DC gain is greater than +200.
10	VCC	Positive power supply: For LVECL operation, connect to V <sub>CC</sub> = 0V. For LVPECL operation, connect to 3.3V. Bypass with 0.1μF    0.01μF low ESR capacitors.

**TRUTH TABLE**

EN	QHG Out	/QHG Out
1	Data	/Data
0	Logic Low	Logic High

### Absolute Maximum Ratings<sup>(1)</sup>

Power Supply Voltage ( $V_{CC} - V_{EE}$ )	+6.0V
PECL Input Voltage ( $V_{IN}$ )	0V to $V_{CC} + 0.5V$
Voltage Applied to Output at High State ( $V_{EE} = 0V$ )	-0.5V to +5.5V
Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Lead Temperature (soldering, 10 sec.)	220°C
Storage Temperature ( $T_S$ )	-65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{IN}$ )	+3.0V to +3.8V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Junction Temperature ( $T_J$ )	160°C
Package Thermal Resistance	
MSOP ( $\theta_{JA}$ )	
Still Air	113°C/W
MSOP ( $\Psi_{JB}$ )	74°C/W

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.0V$  to  $+3.8V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage (LVPECL) (LVECL)	$V_{EE} = GND$	3.0	3.3	3.8	V
		$V_{CC} = GND$	-3.8	-3.3	-3.0	V
$I_{CC}$	Power Supply Current	$V_{CC} = 3.8V$			46	mA
$V_{BB}$	Reference Voltage		$V_{CC} - 1.26$	$V_{CC} - 1.32$	$V_{CC} - 1.38$	V
$I_{IH}$	Input HIGH Current D, /D EN	$V_{IN} = V_{IH} (max)$			150	$\mu A$
		$V_{IN} = V_{CC}$			100	$\mu A$
$I_{IL}$	Input LOW Current D, /D EN	$V_{IN} = V_{IL} (min)$	0.5			$\mu A$
		$V_{IN} = GND$	-300			$\mu A$
$C_{IN}$	Input Capacitance			0.75		pF
EN	Enable	LVECL/LVPECL/CMOS compatible	$V_{EE}$		$V_{CC}$	V

## LVECL/LVPECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.0V$  to  $+3.8V$  and  $V_{EE} = 0V$ ,  $V_{CC} = 0V$  and  $V_{EE} = -3.0V$  to  $-3.8V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ ; unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output High Voltage	$50\Omega$ to $V_{CC} - 2V$	2.215	2.305	2.42	V
$V_{OL}$	Output Low Voltage	$50\Omega$ to $V_{CC} - 2V$	1.470	1.595	1.745	V
$V_{IH}$	Input HIGH Voltage		2.135	—	2.420	V
$V_{IL}$	Input LOW Voltage		1.490	—	1.825	V
$V_{IHCMR}$	Input High Voltage Common Mode Range	<b>Note 3</b>	2.0	—	$V_{CC} - 0.8$	V

**Notes:**

1. Permanent device damage may occur if the ratings in the "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3.  $V_{IHCMR}$  is referenced to the most positive side of the differential input signal.

## AC ELECTRICAL CHARACTERISTICS

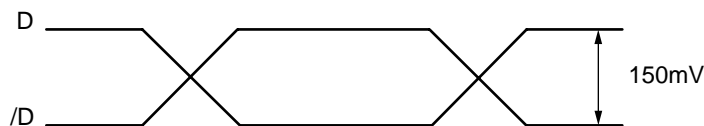
$V_{CC} = +3.0V$  to  $+3.8V$  and  $V_{EE} = GND$  or  $V_{EE} = -3.0V$  to  $-3.8V$  and  $V_{CC} = GND$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Frequency		800			MHz
$t_{pd}$	Propagation Delay (Diff.) to $Q_{FB}$ , $/Q_{FB}$ (Single)				200 230	ps ps
	to $Q_{HG}$ , $/Q_{HG}$ (Diff.) (Single)				730 780	ps ps
$t_S$	Set-Up Time	Enable Pin <sup>(4)</sup>	650			ps
$t_H$	Hold Time	Enable Pin <sup>(4)</sup>	650			ps
$t_{JITTER}$	Cycle-to-Cycle Jitter	RMS		0.2		ps
$t_{SKEW}$	Duty Cycle Skew	<b>Note 5</b>		5	20	ps
$V_{PP}$	Minimum Input Swing	<b>Note 6</b>	150			mV
$t_r$ $t_f$	Output Rise/Fall Times (20% to 80%)	At full output swing			250	ps

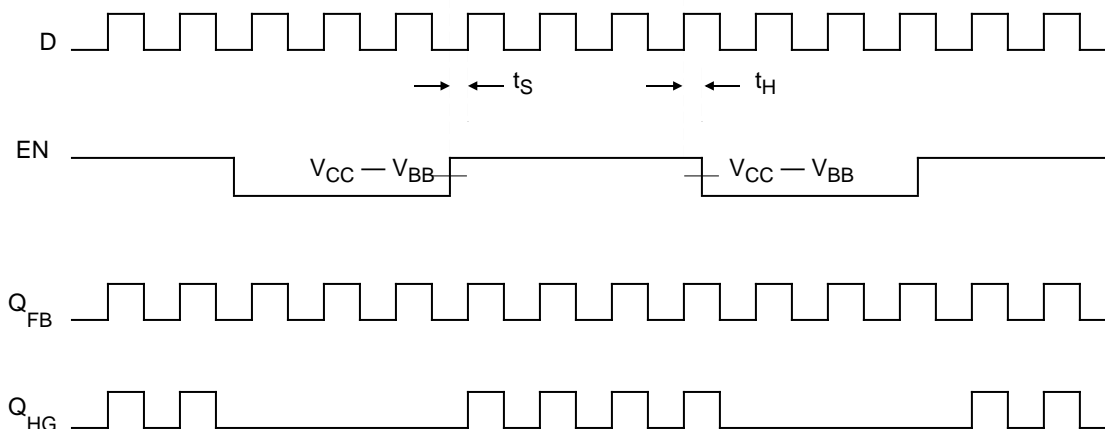
**Notes:**

4. See "Timing Waveform" section.
5. Duty cycle skew is the difference between rise and fall time propagation delay through the device.
6. The device has a DC gain of 10 for Q, /Q outputs, and DC gain of 200 or higher for  $Q_{HG}$ ,  $/Q_{HG}$ . See "Timing Waveform" minimum input swing.

## TIMING WAVEFORMS

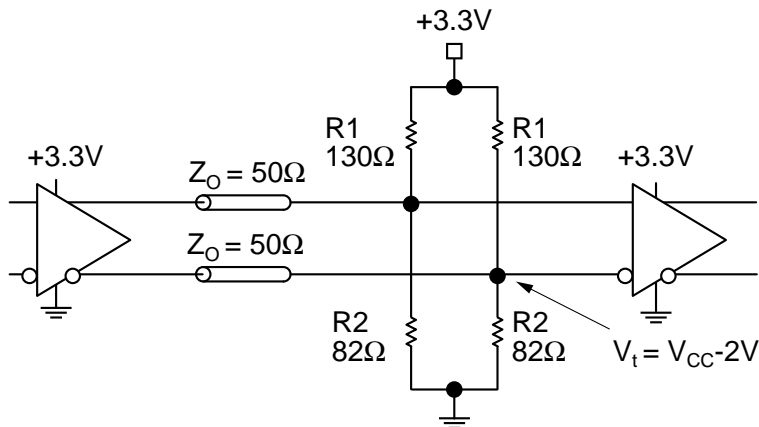


**Figure 1. Minimum Input Swing**

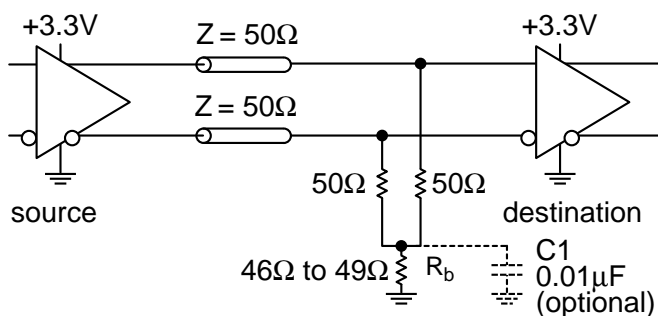


**Figure 2. Set-Up and Hold Timing**

**TERMINATION RECOMMENDATIONS**



**Figure 3. Parallel Termination–Thevenin Equivalent**

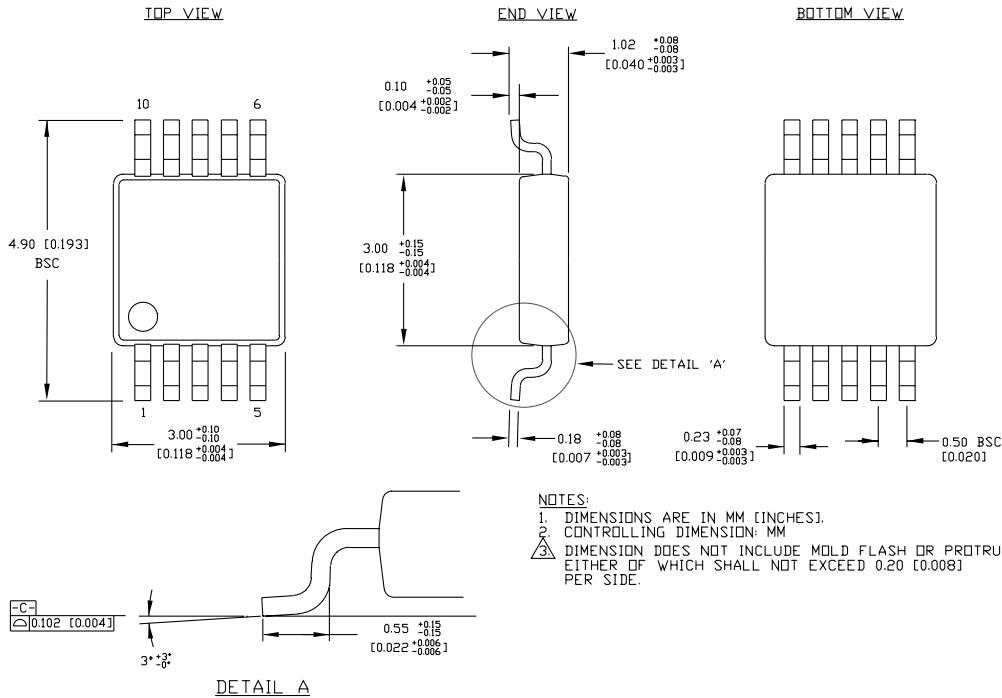


**Figure 4. Three-Resistor ‘Y-Termination’**

**RELATED PRODUCT AND SUPPORT DOCUMENTATION**

Part Number	Function	Data Sheet Link
SY100EL16VO	3.3V/5V 800MHz Precision PECL Amplifier with Low-Gain Feedback	<a href="http://www.micrel.com/product-info/products/sy100el16vo.shtml">www.micrel.com/product-info/products/sy100el16vo.shtml</a>
SY89250V	3.3V/5V Enhanced Differential Receiver	<a href="http://www.micrel.com/product-info/products/sy89250v.shtml">www.micrel.com/product-info/products/sy89250v.shtml</a>

**10 LEAD MSOP (K10-1)**



Rev. 00

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